Reg.No. _____

Karunya UNIVERSITY

(Karunya Institute of Technology & Sciences)
(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

End Semester Examination – Nov/Dec – 2016

Code : 14EC2069
Sub. Name : VLSI Design

Semester : 2016-17 ODD
Duration : 3hrs
Max. marks : 100

ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)

Q. No.	Sub Div.	Questions	Course Outcome	Marks
1.	a.	Explain the different fabrication steps of Silicon On Insulator (SOI) process with neat diagram.	CO1	**12**
	b.	Discuss in detail about Gate array Layout.	CO1	**8**
		(OR)		
2.	a.	Explain in detail about standard cell design.	CO1	**10**
	b.	Explain in detail about Si-gate NMOS fabrication process.	CO1	**10**
3.	a.	With neat diagram, explain the regions of operation of MOS transistor for various terminal voltages.	CO1	**12**
	b.	With small signal model for an MOS transistor derive the small signal AC characteristics.	CO1	**8**
		(OR)		
4.	a.	Obtain the relationship between for Drain-to-source current (I_{ds}) Vs V_{ds} in non-saturation and saturation region.	CO1	**12**
	b.	Explain in detail about Fowler-Nordeim Tunneling,Drain Punchthrough,Mobility and Channel length modulation of MOS transistor.	CO1	**8**
5.	a.	Draw the circuit, stick diagram and the layout of 2-input CMOS NOR Gate.	CO2	**8**
	b.	With neat diagram explain in detail about n-well based CMOS design rules.	CO2	**12**
		(OR)		
6.	a.	Design the following by using CMOS Logic. $F= \overline{((A+B)\,C + D)}$ $F= \overline{(A\,(B\,C + D))}$	CO2	**10**
	b.	Draw the circuit and stick diagram of NMOS NAND Gate.	CO2	**8**
	c.	Give the minimum width and spacing rule of polysilicon.  	CO1	**2**

7.	a.	With neat timing diagram explain in detail about np-CMOS logic.	CO2	**8**
	b.	Explain in detail about CMOS Domino logic and draw the following expression using the same. (Z= A.B+ C.D)	CO2	**12**
		(OR)		
8.	a.	With neat diagram explain in detail about **clocked CMOS** logic (C^2MOS) and design 3-input NAND gate using **clocked CMOS** (C^2MOS) logic.	CO2	**12**
	b.	Design $Z=((A.B.C)+D)$ using pseudo NMOS logic.	CO3	**8**
		Compulsory:		
9.	a.	Explain in detail about Dynamic CMOS logic and design the following Boolean expression using Dynamic CMOS Logic. $F=(A1.A2.A3)+(B1.B2)$	CO2	**14**
	b.	Design $Z = AB + (C + D)(E + F)$ using CMOS logic.	CO3	**6**

ALL THE BEST